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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,881	11/05/2003	Robert A. Guenther	200309963-1	6718

22879 7590 12/15/2006

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EXAMINER	
PARRIES, DRU M	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,881	GUENTHER ET AL.	
	Examiner	Art Unit	
	Dru M. Parries	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed June 8, 2006 have been fully considered but they are not persuasive. To clarify, the Examiner misread Fig. 1 of the current application, and obviously, the intermediate bus was misinterpreted as numeral 130, and the Examiner, obviously, meant it to be numeral 100. Regarding the arguments of claims 1, 11, 17, and 24, interpreting the intermediate bus limitation broadly, saying "to supply independent and redundant input to a second set of power converters", the Examiner believes Fig. 1 reads on this because each second converter (110 of Fig. 1) receives one (independent) input into it, and the input is redundant because each converter is getting the same input value. Also, the term "interleaved" in regards to a bus is vague; the Examiner believes that the bus structure in Fig. 1 would read on "interleaved" (according to Webster's dictionary it means, "to arrange in layers"). One could say there are three layers of the bus in Fig. 1, each layer for each of the three different output voltages from the second converters.

Regarding claims 5, 12, and 21, simple rearranging of parts (i.e. wiring of the bus) involves only routine skill in the art. *In re Japikse*, 86 USPQ 70. The motivation to do this is, in the case of malfunction of one of the first power converters, one can eliminate the need for the diodes (130) and therefore save cost, and it won't negatively affect the inputs to *all* the second power converters. Another motivation to do this is so that each set of corresponding first and second converters (via independent bus) can act independently of other sets of first and second converters to output the most precise voltage with the least amount of outside interference as possible.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3-4, 7, 11, 17, 24-25, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Prior Art (Admission). Admission teaches a power source (+48V), a first set of isolated converters (105), a plurality of subsets of non-isolated converters (110) and an interleaved intermediate bus (130) to supply independent and redundant input to the second set of converters from the first set of converters. (Fig. 1)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 6, 12-15, 20-23, 26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art (Admission). Admission teaches a power source (+48V), a first set of isolated converters (105), a plurality of subsets of non-isolated converters (110) and an interleaved intermediate bus (130) to supply independent and redundant input to the second set

of converters from the first set of converters. (Fig. 1) Admission fails to teach the intermediate bus configured without fault protection components. It would have been obvious to one of ordinary skill in the art at the time of the invention to omit the fault protection components from the intermediate bus, since it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson*, 136 USPQ 184. Admission also fails to teach the intermediate bus forming multiple independent buses and connecting each bus as a one-to-one relationship with each converter in each of the plurality of subsets of converters. It would have been obvious to one of ordinary skill in the art at the time of the invention to form the intermediate bus into multiple independent buses and connecting each bus as a one-to-one relationship with each converter in each of the plurality of subsets of converters, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70. It also would have been obvious because each set of corresponding first and second converters (via independent bus) can act independently of other sets of first and second converters so that they will be able to output the most precise voltage with the least amount of outside interference as possible, and it would also eliminate the need for the protection diodes, and therefore save money.

6. Claims 2 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art (Admission) as applied to claims 1, 11, and 13 above, and further in view of De Rooij et al. (2004/0125618). Admission teaches the power distribution system described above. Admission fails to explicitly teach what is inside the power converters. De Rooij teaches a power converter comprising a power transformer. It would have been obvious to one of ordinary skill in the art at

the time of the invention to incorporate a power transformer into all of the converters in Admission because De Rooij teaches converters comprising transformers and Admission is silent as to what the converter comprises.

7. Claims 8-10, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art (Admission) as applied to claims 1 and 17 above, and further in view of Barnsdale, Jr. et al. (4,685,056). Admission teaches the power distribution system described above. Admission also teaches the non-isolated converters being selectively combined to generate one or more selected output levels. Admission fails to explicitly teach the system being embedded into a computer system and supplying output power to logic devices. Barnsdale teaches a power supply system embedded in a computer system, and supplies power to logic devices (Abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention to place Admission's power distribution system into the computer system of Barnsdale because it is shown that power needs to be supplied to computer systems and Admission's system would be a good system to supply that power due to the multiple output power levels that could be used for various logic devices needing different supply voltages.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dru M. Parries whose telephone number is (571) 272-8542. The examiner can normally be reached on M-Th from 9:00am to 6:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMP

12-7-2006

CHAU N. NGUYEN
PRIMARY EXAMINER